AMENDMENTS TO THE CLAIMS

Please add new claims 14-20 as shown in the following list of claims.

1. (Original) An integrated circuit on a chip, comprising:

a substrate; and

at least one scan chain disposed in the substrate, with scan cells connected to form a series chain, each connection being formed according to a layout constraint with a minimum dimension provided by design rules for an assigned routing layer.

2. (Original) The integrated circuit as claimed in claim 1, wherein the assigned routing layer is a first metal layer.

3. (Original) The integrated circuit as claimed in claim 2, wherein the layout constraint limits the connection to passage through at least the first metal layer.

4. (Original) The integrated circuit as claimed in claim 3, wherein the layout constraint limits the connection to passage through only the first metal layer.

5. (Original) The integrated circuit as claimed in claim 3, wherein the layout constraint limits each metal line of the first metal layer, to form the connection, to line width of critical dimension (CD) of the first metal layer.

6. (Original) The integrated circuit as claimed in claim 3, wherein the layout constraint further limits any metal line of a second metal layer in the connection to a line width exceeding CD of the second metal layer.

7. (Original) The integrated circuit as claimed in claim 3, wherein the layout constraint further requires any plug of a plug layer linking two metal lines in the connection to be more than one.

8. (Original) The integrated circuit as claimed in claim 1, wherein the assigned routing layer is a plug layer.

9. (Original) The integrated circuit as claimed in claim 8, wherein the layout constraint limits the connection to passage through at least the plug layer and plugs of the plug layer, linking two metal lines in the connection, to one only.

10. (Original) The integrated circuit as claimed in claim 9, wherein the layout constraint further limits any metal line of a metal layer in the connection to a line width exceeding CD of the metal layer.

11. (Original) The integrated circuit as claimed in claim 1, wherein the integrated circuit further has an auxiliary routing net positioned in parallel beside the scan chain, the auxiliary routing net has metal lines of different lengths, and the auxiliary routing net does not function when the scan chain is originally formed.

12. (Original) The integrated circuit as claimed in claim 11, wherein one of the metal lines has sufficient length to replace one of the connections in the scan chain.

13. (Original) The integrated circuit as claimed in claim 11, wherein one of the metal lines has a length equal to at least two scan cells in the scan chain.

14. (New) An integrated circuit on a chip, comprising:

a substrate; and

at least one scan chain disposed on the substrate, with scan cells connected by connecting lines to form a series chain, each connecting line being formed according to a layout constraint with a minimum dimension provided by design rules for an assigned routing layer.

15. (New) The integrated circuit as claimed in claim 14, wherein the assigned routing layer is a first metal layer.

16. (New) The integrated circuit as claimed in claim 15, wherein the layout constraint requires at least one connecting line to traverse at least the first metal layer.

17. (New) The integrated circuit as claimed in claim 16, wherein the layout constraint requires the at least one connecting line to traverse only the first metal layer.

18. (New) The integrated circuit as claimed in claim 16, wherein the layout constraint requires each metal line of the first metal layer, forming the at least one connecting line, to have a line width of a critical dimension for the first metal layer.

19. (New) The integrated circuit as claimed in claim 16, wherein the layout constraint further requires any metal line of a second metal layer, forming the at least one connecting line, to have a line width exceeding a critical dimension for the second metal layer.

20. (New) The integrated circuit as claimed in claim 16, wherein the layout constraint further requires any plug connection of a plug layer linking two metal lines forming the at least one connecting line to be more than one plug.